In the claims:

1. (Cancelled) A method of designing an integrated circuit, comprising:

identifying a programmable logic core;

identifying an application;

designing an application specific circuit for the application; and

integrating the programmable logic core into the designed application specific circuit.

2. (Cancelled) A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a set of timing constraints associated with the programmable logic core; and

controlling the design of application specific circuitry that interfaces with the programmable logic core in the integrated circuit in accordance with the set of timing constraints.

3. (Cancelled) A method of designing an integrated circuit, comprising:

identifying a programmable logic core for the integrated circuit;

establishing a sign-off design associated with the programmable logic core; and

controlling the design of application specific circuitry that interfaces with the programmable logic core in the integrated circuit in accordance with the sign-off design.

4. (Cancelled) An integrated circuit, comprising;

a programmable logic core; and

application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design.

5. (Cancelled) An integrated circuit according to claim 4, wherein the programmable logic core includes:

a programmable multi-scale array;

an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry; and

a programmable logic core adapter that configures the programmable multi-scale array.

6. (Cancelled) The integrated circuit of claim 5, wherein the programmable multi-scale array comprises an array of configurable arithmetic logic units supporting at least:

register transfer level functions; and

random logic structures.

7. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core comprises a programmable multi-scale array supporting functions of different scales.

8. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core includes at a programmable logic core control for loading configuration data into the programmable logic core.

9. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core comprises:

an array of configurable logic structures having internal storage registers; and

a scratchpad memory to supplement the storage registers.

10. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core includes at a configuration test interface for data and control flow between the application specific circuit and the programmable logic core.

11. (Cancelled) The integrated circuit according to claim 4 further comprising a microprocessor core communicatively connected to the programmable logic core.

12. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core comprises blocks supporting:

configuration data control logic;

scan path logic; and

application circuit interface logic.

13. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic core comprises arithmetic logic units including:

function cells; and

an arithmetic logic unit controller.

14. (Cancelled) The integrated circuit according to claim 4, wherein the programmable logic comprises:

an internet protocol core; and

arithmetic logic units communicatively connected to the internet protocol core.

15. (Previously presented) An integrated circuit, comprising:

a programmable logic core that supports:

an idle state that is entered after an assertion of a signal that power is good;

a built in self test state for testing the programmable logic core, the built in self test state is entered from the idle state upon receipt of a test command;

a configuration state for implementing a configuration process, the configuration state supports entry from the idle state and from the built in self test state after receipt of a configuration clock signal; and

an operate state that controls operations of arithmetic logic units, and is entered after completion of the configuration process; and

application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design.

16. (Cancelled) An integrated circuit, comprising;

means for performing functions associated with a programmable logic core; and

means for performing functions associated with application specific circuitry that is designed in accordance with a sign-off design.

17. (Previously Presented) An integrated circuit, comprising:

(I) application specific circuitry, the application specific circuitry being designed in accordance with a sign-off design; and

(II) a first programmable logic core including at least

(A) a programmable multi-scale array having an array of configurable arithmetic logic units supporting register transfer level functions, random logic structures, and state machine structures,

(B) an application circuit interface for providing a signal interface between the programmable multi-scale array and the application specific circuitry, the application circuit interface having test registers for testing the programmable logic core,

(C) scratchpad memories for supplementing storage of the programmable multi-scale array,

(D) a configuration test interface for data and control flow between the application specific circuit and the programmable multi-scale array,

(E) a programmable logic control for loading configuration data into the multi-scale array, and

(F) a programmable logic core adapter that configures the programmable multi-scale array through the configuration test interface.

19. (Previously presented) The integrated circuit according to claim 15, wherein the first programmable logic core comprises:

a programmable multi-scale array comprising a plurality of configurable arithmetic logic units; and

a programmable logic core adapter that configures the programmable multi-scale array.

20. (Previously presented) The integrated circuit according to claim 15, wherein the programmable logic core adapter is configured to receive configuration data and load the configuration data into configuration memory of the programmable logic core adapter.

21. (Previously presented) The integrated circuit according to claim 15, wherein the first programmable logic core comprises an application circuit interface that interfaces between the programmable multi-scale array and the application specific circuitry.

22. (Previously presented) The integrated circuit according to claim 15, wherein the programmable multi-scale array performs register transfer level functions.

23. (Previously presented) The integrated circuit according to claim 15, further comprising a plurality of other programmable logic cores.

24. (Previously presented) The integrated circuit according to claim 15, wherein the first programmable logic core includes a programmable logic core control for controlling the programmable logic core.

25. (Previously presented) The integrated circuit according to claim 24, wherein the programmable logic core control provides a control mechanism for testing the first programmable logic core.

26. (Previously presented) The integrated circuit according to claim 15, further comprising scratchpad memory.

27. (Previously presented) The integrated circuit according to claim 17, further comprising a configuration data source that stores the configuration data.

28. (Previously presented) The integrated circuit according to claim 17, further comprising a plurality of other programmable logic cores.

29. (Previously presented) The integrated circuit according to claim 17, wherein the programmable logic core control provides a control mechanism for testing the first programmable logic core.